Remarks

As discussed below, the rejections of claims 1-16 cannot be maintained because they are predicated on a mischaracterization of the two-miss allocation approach taught by the Sherwood reference. In particular, the cited portions of the Sherwood reference are not arranged as required by the claimed invention and thus the rejections violate M.P.E.P. § 2131, which states that the elements of a reference must be arranged as required by the claim.

The instant Office Action dated November 20, 2008, listed the following rejections: claims 1-2, 4-8, 10-14 and 16 stand rejected under 35 U.S.C. § 102(b) over Sherwood *et al.* ("Predictor-Directed Stream Buffers); and claims 3, 9 and 15 stand rejected under 35 U.S.C. § 103(a) over Sherwood in view of Handy (the Cache Memory Book). The Office Action notes an objection to claim 16 under 37 CFR 1.75 as being a duplicate of claim 2. Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant respectfully traverses the § 102(b) rejection of claims 1-2, 4-8, 10-14 and 16 because the rejection relies upon an erroneous interpretation of the cited portions of the Sherwood reference. The claimed invention includes aspects directed to accessing and updating a stride prediction table (SPT) only when a cache miss occurs, which are not taught by the cited portions of Sherwood. Instead, the cited portions of the Sherwood reference teach that two-miss allocation filter allows a load to allocate a stream buffer (*i.e.*, the Examiner's alleged cache memory circuit) when the load has two cache misses in a row. *See, e.g.*, Fig. 3 and Sec. 4.3. The cited portions of Sherwood do not teach accessing and updating stride predictor (*i.e.*, the Examiner's alleged SPT) when the load has two cache misses in a row. As such, the cited portions of the Sherwood reference are not arranged as required by the claimed invention. *See, e.g.*, M.P.E.P. § 2131. Applicant notes that Sherwood states "(w)hen updating the SFM predictor for a load that missed in the cache, both the PC-based stride table and the address based Markov table are indexed, and potentially updated"; however, Sherwood does not teach that the PC-based stride table is indexed and potentially updated only when a cache miss is detected as in the claimed invention. *See, e.g.*, Fig. 3 and Sec. 4.3. Thus, the cited portions of the Sherwood reference

do not correspond to the claimed invention. Accordingly, the § 102(b) rejection of claims 1-2, 4-8, 10-14 and 16 is improper and Applicant request that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claims 1-2, 4-8 and 10 because the Examiner fails to identify what component of the Sherwood reference is being asserted as allegedly corresponding to Applicant's first memory circuit. Instead, the Examiner simply cites to Fig. 3 of Sherwood with no further explanation regarding the alleged correspondence. In fact, Fig. 3 of Sherwood shows 8 buffers (stream buffers), the Examiner's alleged cache memory circuit, which are apparently connected to several additional components (*e.g.,* next lower level of memory, data cache and register file) that are not shown in Fig. 3. In order to comply with 35 U.S.C. § 132, sufficient detail must be provided by the Examiner regarding the alleged correspondence between the claimed invention and the cited reference to enable Applicant to adequately respond to the rejections. *See, also,* 37 CFR 1.104 ("The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.") and M.P.E.P. § 706.02(j), ("It is important for an Examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply."). As such, Applicant requests clarification, by way of a new Office Action, regarding what component of the Sherwood reference is being asserted as allegedly corresponding to Applicant's first memory circuit. *See, e.g.,* M.P.E.P. § 706.07 "The examiner should never lose sight of the fact that in every case the applicant is entitled to a full and fair hearing, and that a clear issue between applicant and examiner should be developed, if possible, before appeal."). Without such clarification, Applicant submits that the § 102(b) rejection of claims 1-2, 4-8 and 10 is improper and cannot be maintained.

Applicant further traverses the § 102(b) rejection of claim 4 because the cited portions of the Sherwood reference do not correspond to aspects of the claimed invention directed to the cache memory circuit and the SPT being within the same physical memory space. Fig. 3 of Sherwood shows that the stream buffers or the 8 buffers (*i.e.,* the Examiner's alleged cache memory circuit) is separate from the stride predictor (*i.e.,* the Examiner's alleged SPT) and the cited portions of Sherwood do not teach that the stream buffers and the stride predictor are within the same physical memory space as in the claimed

invention. Accordingly, the § 102(b) rejection of claim 4 is improper and Applicant request that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claim 10 because the cited portions of the Sherwood reference do not correspond to aspects of the claimed invention directed to the SPT comprising an address filed having a size that is less than the address space used to index the SPT. Instead, the cited portions of the Sherwood reference discuss storing partial addresses tags in the Markov table (or Markov predictor shown in Fig. 3), without providing an indication of the size of an address field in the stride predictor (*i.e.,* the Examiner's alleged SPT). As such, the cited portions of the Sherwood reference are once again not arranged as required by the claimed invention. *See, e.g.,* M.P.E.P. § 2131. Moreover, the cited portions of Sherwood do not provide any teachings that the size of an address field in the stride predictor is less than the address space used to index the stride predictor as in the claimed invention. Accordingly, the § 102(b) rejection of claim 10 is improper and Applicant request that it be withdrawn.

Applicant respectfully traverses the § 103(a) rejection of claims 3, 9 and 15 because the rejection relies upon the aforementioned misinterpretation of the Sherwood reference. Moreover, the Examiner fails to provide any reason why the skilled artisan would modify the Sherwood reference. Instead, the Examiner simply states that it would have been obvious "to implement the circuit construction concepts as taught by Handy in the system of Sherwood because they are notoriously well known concepts in the art." This approach is contrary to the requirements of § 103 and relevant law. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007). ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). The Examiner still must provide a reason/motivation for why the skilled artisan would implement the teachings of Handy in the system of Sherwood. As no such reason has been presented by the Examiner, the § 103(a) rejection of claims 3, 9 and 15 necessarily fails and must be withdrawn.

Applicant respectfully traverses the objection to claim 16 under 37 CFR 1.75 as being a duplicate of claim 2 because, as stated by the Examiner, "it is proper after allowing one claim to objection to the other as being a substantial duplicate of the allowed claim." *See, e.g.,* M.P.E.P. § 706.03(k). As claim 2 has not been allowed, the objection to claim 16 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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